



IEEE Asian Solid-State Circuits Conference

November 18 - 21, 2024
International Conference Center Hiroshima, Japan

Sponsors Opportunities

The IEEE A-SSCC (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society.

IEEE A-SSCC 2024 will be held in Hiroshima, Japan on November 18-21, 2024. The conference will start with a one-day tutorial session on November 18 and plenary talks is scheduled at the start of the main program, November 19 through 21. The main program includes contributed presentations, panel discussion, Student Design Contest exhibition and FPGA demo sessions.

We hope that you will support the purpose of the conference and joins us as sponsors.

A-SSCC History

2005	Taiwan
2006	China
2007	Korea
2008	Fukuoka, Japan
2009	Taiwan
2010	China
2011	Korea
2012	Kobe, Japan
2013	Singapore
2014	Taiwan
2015	China
2016	Toyama, Japan
2017	Korea
2018	Taiwan
2019	Macao
2020	Japan (Online)
2021	Korea
2022	China
2023	China
2024	Hiroshima, Japan

Conference Scope

1. Analog Circuits & Systems: Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.

2. Data Converters: Nyquist-rate and oversampling A/D, D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.

3. Digital Circuits & Systems: Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.

4. SoC & Signal Processing Systems: System-on-chip (including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.

5. Wireless: Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.

6. Wireline: Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.

7. Emerging Technologies and Applications: Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; silicon photonics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design, artificial intelligent system, and cryogenic circuits and systems.

8. Memory: Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.

9. FPGA: Novel algorithm and/or architecture for integrated circuits validated by FPGA implementation. The authors of accepted papers are required to participate in demo sessions.



About A-SSCC 2024

- Conference Name: IEEE Asian Solid-State Circuits Conference 2024 (A-SSCC 2024)
- Sponsored by : IEEE SSCS (Solid-State Circuits Society)
- Date : Monday, November 18 – 21, 2024 (four days)
- Venue : International Conference Center Hiroshima, Hiroshima, Japan [Access](#)
- Participants (Est.) :400
- Proceedings : Online proceedings at D/L site

IMPORTANT DATES

- Paper submission due: June 10, 2024, 20:00 (GMT)
- Paper selection meeting: July 26, 2024
- Acceptance notification: August 9, 2024
- Final paper submission: September 12, 2024

SCHEDULE FOR SPONSORS

- Sponsorship application due: June 30, 2024

A-SSCC 2024 Committee

Steering Committee

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A-SSCC 2024 provides a variety of options for sponsor packages. The benefits of each package are summarized below.

	Platinum	Gold	Silver
Complimentary registration	5	3	1
Logo on conference website/materials	✓	✓	✓
1 page Ad included in the conference program	✓	✓	✓
Logo on screen saver in session rooms	✓	✓	✓
Logo on vertical banner in the conference venue	✓	✓	✓
Sponsored Session**	✓		
1-min PR movie prior to one plenary speech	✓	✓	
	¥1,000,000	¥500,000	¥300,000

* All rates are shown exclusive of tax.

About Sponsored Session:

Date: 50 minutes (1 slot) in 16:00-18:00 on November 19 and 20, 2024.
16:00-16:50, 17:00-17:50, November 19 and 20, 2024.

Location: Hiroshima International Conference Center, B1F

Room capacity: Theater style, 60 people

Room (screen, projector, 2 microphones and speakers included) will be provided.

Program schedule planning, promotion, and operation are the responsibility of the sponsors.

Requests for additional equipment can be accommodated at an additional cost.

Contact:

A-SSCC 2024 Secretariat

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<https://a-sscc2024.org/>